Amendments to the Specification:

Please replace the paragraph beginning on page 4, line 18, with the following

amended paragraph:

The host microprocessor 20 writes the transfer-based transfer descriptors into the

RAM 50 or 58-56 of the host controller 40 through the peripheral bus 32, without the

host controller 40 requiring to master the bus 32. In other words, the host controller 40

acts only as a slave. The transfer-based transfer descriptors can then be memory-mapped

into the RAM 50 or 58-56 of the host controller 40.

Please replace the paragraph beginning on page 4, line 23, with the following

amended paragraph:

Advantageously, the built-in memory 50 or 58-56 of the host controller 40 is

mapped in the host microprocessor 20, improving the ease with which transactions can

be scheduled from the host microprocessor 20.

Please replace the paragraph beginning on page 5, line 3, with the following

amended paragraph:

The transfer-based protocol allows the host microprocessor 20 to write a 1ms

frame of data into the RAM 50 or  $58-\underline{56}$  of the host controller (provided that the RAM is

large enough to hold this data), such that this can be transmitted over the USB bus  $42\,$ 

without further intervention from the host microprocessor  $\underline{20}.$ 

Attorney Docket No. NL 030575 US1 Serial No. 10/556,450

2

Amendment and Response to Office Action